

Refine Search

Search Results -

Terms	Documents
(709/253 716/16 716/17 370/402 370/465 712/32 712/37 712/41 710/1 710/8 710/105 710/305 710/2 710/104 710/306 326/37 326/38 326/39).ccls.	10961

Database:

- US Pre-Grant Publication Full-Text Database
- US Patents Full-Text Database
- US OCR Full-Text Database
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Search:

L1

Refine Search

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Search History

DATE: Friday, June 03, 2005 [Printable Copy](#) [Create Case](#)

<u>Set</u> <u>Name</u> side by side	<u>Query</u>	<u>Hit</u> <u>Count</u>	<u>Set</u> <u>Name</u> result set
	<i>DB=PGPB,USPT,USOC; PLUR=YES; OP=OR</i>		
<u>L1</u>	710/1,8,105,305,2,104,306;716/16,17;712/32,37,41;326/37-39;370/402,465;709/253.ccls.	10961	<u>L1</u>

END OF SEARCH HISTORY

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Database:

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Search:

L7

Search History

DATE: Friday, June 03, 2005 [Printable Copy](#) [Create Case](#)

<u>Set</u> <u>Name</u> side by side	<u>Query</u>	<u>Hit</u> <u>Count</u>	<u>Set</u> <u>Name</u> result set
	DB=PGPB,USPT,USOC; PLUR=YES; OP=OR		
<u>L7</u>	l1 and L6	30	<u>L7</u>
<u>L6</u>	l4 same bus	166	<u>L6</u>
<u>L5</u>	l1 and L4	161	<u>L5</u>
<u>L4</u>	l2 same configur\$4	730	<u>L4</u>
<u>L3</u>	l1 and L2	382	<u>L3</u>
<u>L2</u>	"programmable logic device" same (processor or microprocessor or (micro adj1 processor))	6825	<u>L2</u>
<u>L1</u>	710/1,8,105,305,2,104,306;716/16,17;712/32,37,41;326/37-39;370/402,465;709/253.ccls.	10961	<u>L1</u>

END OF SEARCH HISTORY

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☐ 1. Document ID: US 20050114553 A1

L7: Entry 1 of 30

File: PGPB

May 26, 2005

PGPUB-DOCUMENT-NUMBER: 20050114553

PGPUB-FILING-TYPE: new

DOCUMENT-IDENTIFIER: US 20050114553 A1

TITLE: Handheld option pack interface

PUBLICATION-DATE: May 26, 2005

INVENTOR-INFORMATION:

NAME	CITY	STATE	COUNTRY	RULE-47
Lada, Henry F.	Cypress	TX	US	
Mann, James M.	Cypress	TX	US	

US-CL-CURRENT: 710/1

Full	Title	Citation	Front	Review	Classification	Date	Reference	Sequences	Attachments	Claims	RMC	Draw Desc	Image
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☐ 2. Document ID: US 20050097499 A1

L7: Entry 2 of 30

File: PGPB

May 5, 2005

PGPUB-DOCUMENT-NUMBER: 20050097499

PGPUB-FILING-TYPE: new

DOCUMENT-IDENTIFIER: US 20050097499 A1

TITLE: In-circuit configuration architecture with non-volatile configuration store for embedded configurable logic array

PUBLICATION-DATE: May 5, 2005

INVENTOR-INFORMATION:

NAME	CITY	STATE	COUNTRY	RULE-47
Sun, Albert	Hsinchu		TW	
Sheu, Eric	Hsinchu		TW	
Chen, Shih-Liang	Fengyuan		TW	

US-CL-CURRENT: 716/16

Full	Title	Citation	Front	Review	Classification	Date	Reference	Sequences	Attachments	Claims	RMC	Draw Desc	Image
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☐ 3. Document ID: US 20050093572 A1

L7: Entry 3 of 30

File: PGPB

May 5, 2005

PGPUB-DOCUMENT-NUMBER: 20050093572

PGPUB-FILING-TYPE: new

DOCUMENT-IDENTIFIER: US 20050093572 A1

TITLE: In-circuit configuration architecture with configuration on initialization function for embedded configurable logic array

PUBLICATION-DATE: May 5, 2005

INVENTOR-INFORMATION:

NAME	CITY	STATE	COUNTRY	RULE-47
Sun, Albert	Hsinchu		TW	
Sheu, Eric	Hsinchu		TW	
Chen, Shih-Liang	Hsinchu		TW	

US-CL-CURRENT: 326/38; 326/41, 326/47

Full	Title	Citation	Front	Review	Classification	Date	Reference	Sequences	Attachments	Claims	K00C	Draw Desc	Image
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☐ 4. Document ID: US 20040155676 A1

L7: Entry 4 of 30

File: PGPB

Aug 12, 2004

PGPUB-DOCUMENT-NUMBER: 20040155676

PGPUB-FILING-TYPE: new

DOCUMENT-IDENTIFIER: US 20040155676 A1

TITLE: Fracturable incomplete look up table for area efficient logic elements

PUBLICATION-DATE: August 12, 2004

INVENTOR-INFORMATION:

NAME	CITY	STATE	COUNTRY	RULE-47
Kaptanoglu, Sinan	Belmont	CA	US	
Lewis, David	Toronto	CA	CA	
Pedersen, Bruce	San Jose		US	

US-CL-CURRENT: 326/38

Full	Title	Citation	Front	Review	Classification	Date	Reference	Sequences	Attachments	Claims	K00C	Draw Desc	Image
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☐ 5. Document ID: US 20040113655 A1

L7: Entry 5 of 30

File: PGPB

Jun 17, 2004

PGPUB-DOCUMENT-NUMBER: 20040113655

PGPUB-FILING-TYPE: new

DOCUMENT-IDENTIFIER: US 20040113655 A1

TITLE: Partial reconfiguration of a programmable logic device using an on-chip processor

PUBLICATION-DATE: June 17, 2004

INVENTOR-INFORMATION:

NAME	CITY	STATE	COUNTRY	RULE-47
Curd, Derek R.	Woodside	CA	US	
Kalra, Punit S.	Superior	CO	US	
LeBlanc, Richard J.	Longmont	CO	US	
Eck, Vincent P.	Loveland	CO	US	
Trynosky, Stephen W.	Boulder	CO	US	
Lindholm, Jeffrey V.	Longmont	CO	US	
Bauer, Trevor J.	Boulder	CO	US	

US-CL-CURRENT: 326/40; 326/41, 716/16

Full	Title	Citation	Front	Review	Classification	Date	Reference	Sequences	Attachments	Claims	KWIC	Draw Desc	Image
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☐ 6. Document ID: US 20040030861 A1

L7: Entry 6 of 30

File: PGPB

Feb 12, 2004

PGPUB-DOCUMENT-NUMBER: 20040030861

PGPUB-FILING-TYPE: new

DOCUMENT-IDENTIFIER: US 20040030861 A1

TITLE: Customizable computer system

PUBLICATION-DATE: February 12, 2004

INVENTOR-INFORMATION:

NAME	CITY	STATE	COUNTRY	RULE-47
Plackle, Bart	Diest		BE	
Herremans, Kurt	Hasselt		BE	

US-CL-CURRENT: 712/32

Full	Title	Citation	Front	Review	Classification	Date	Reference	Sequences	Attachments	Claims	KWIC	Draw Desc	Image
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☐ 7. Document ID: US 20030196021 A1

L7: Entry 7 of 30

File: PGPB

Oct 16, 2003

PGPUB-DOCUMENT-NUMBER: 20030196021

PGPUB-FILING-TYPE: new

DOCUMENT-IDENTIFIER: US 20030196021 A1

TITLE: Method for message transmission exploiting unused device addresses

PUBLICATION-DATE: October 16, 2003

INVENTOR-INFORMATION:

NAME	CITY	STATE	COUNTRY	RULE-47
Botchek, Robert	Saratoga	CA	US	

US-CL-CURRENT: 710/315; 710/104

Full	Title	Citation	Front	Review	Classification	Date	Reference	Sequences	Attachments	Claims	KMIC	Draw Desc	Image
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☐ 8. Document ID: US 20030160633 A1

L7: Entry 8 of 30

File: PGPB

Aug 28, 2003

PGPUB-DOCUMENT-NUMBER: 20030160633

PGPUB-FILING-TYPE: new

DOCUMENT-IDENTIFIER: US 20030160633 A1

TITLE: PROGRAMMING CIRCUITS AND TECHNIQUES FOR PROGRAMMABLE LOGIC

PUBLICATION-DATE: August 28, 2003

INVENTOR-INFORMATION:

NAME	CITY	STATE	COUNTRY	RULE-47
Terrill, Richard Shaw	Sunnyvale	CA	US	
Bielby, Robert Richard Noel	Fremont	CA	US	

US-CL-CURRENT: 326/39

Full	Title	Citation	Front	Review	Classification	Date	Reference	Sequences	Attachments	Claims	KMIC	Draw Desc	Image
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☐ 9. Document ID: US 20030122577 A1

L7: Entry 9 of 30

File: PGPB

Jul 3, 2003

PGPUB-DOCUMENT-NUMBER: 20030122577

PGPUB-FILING-TYPE: new

DOCUMENT-IDENTIFIER: US 20030122577 A1

TITLE: PROGRAMMABLE LOGIC CONFIGURATION DEVICE WITH CONFIGURATION MEMORY ACCESSIBLE TO A SECOND DEVICE

PUBLICATION-DATE: July 3, 2003

INVENTOR-INFORMATION:

NAME	CITY	STATE	COUNTRY	RULE-47
Veenstra, Kerry S.	San Jose	CA	US	
Ang, Boon-Jin	Penang		MY	

US-CL-CURRENT: 326/38

Full	Title	Citation	Front	Review	Classification	Date	Reference	Sequences	Attachments	Claims	KMIC	Draw Desc	Image
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☐ 10. Document ID: US 20030020512 A1

L7: Entry 10 of 30

File: PGPB

Jan 30, 2003

PGPUB-DOCUMENT-NUMBER: 20030020512

PGPUB-FILING-TYPE: new

DOCUMENT-IDENTIFIER: US 20030020512 A1

TITLE: System and method for in-system programming through an on-system JTAG bridge of programmable logic devices on multiple circuit boards of a system

PUBLICATION-DATE: January 30, 2003

INVENTOR-INFORMATION:

NAME	CITY	STATE	COUNTRY	RULE-47
Mantey, Paul	Ft. Collins	CO	US	
Erickson, Mike	Loveland	CO	US	
Maciorowski, David	Parker	CO	US	

US-CL-CURRENT: 326/38; 326/39

Full	Title	Citation	Front	Review	Classification	Date	Reference	Sequences	Attachments	Claims	KWC	Draw Desc	Image
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☐ 11. Document ID: US 6892267 B2

L7: Entry 11 of 30

File: USPT

May 10, 2005

US-PAT-NO: 6892267

DOCUMENT-IDENTIFIER: US 6892267 B2

TITLE: Method for message transmission exploiting unused device addresses

Full	Title	Citation	Front	Review	Classification	Date	Reference			Claims	KWIC	Draw Desc	Image
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☐ 12. Document ID: US 6888373 B2

L7: Entry 12 of 30

File: USPT

May 3, 2005

US-PAT-NO: 6888373

DOCUMENT-IDENTIFIER: US 6888373 B2

TITLE: Fracturable incomplete look up table for area efficient logic elements

Full	Title	Citation	Front	Review	Classification	Date	Reference			Claims	KWIC	Draw Desc	Image
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☐ 13. Document ID: US 6862724 B1

L7: Entry 13 of 30

File: USPT

Mar 1, 2005

US-PAT-NO: 6862724

DOCUMENT-IDENTIFIER: US 6862724 B1

TITLE: Reconfigurable programmable logic system with peripheral identification data

Full	Title	Citation	Front	Review	Classification	Date	Reference			Claims	KWIC	Draw Desc	Image
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☐ 14. Document ID: US 6760888 B2

L7: Entry 14 of 30

File: USPT

Jul 6, 2004

US-PAT-NO: 6760888

DOCUMENT-IDENTIFIER: US 6760888 B2

TITLE: Automated processor generation system for designing a configurable processor and method for the same

Full	Title	Citation	Front	Review	Classification	Date	Reference			Claims	KWIC	Draw Desc	Image
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☐ 15. Document ID: US 6748457 B2

L7: Entry 15 of 30

File: USPT

Jun 8, 2004

US-PAT-NO: 6748457

DOCUMENT-IDENTIFIER: US 6748457 B2

TITLE: Data storewidth accelerator

Full	Title	Citation	Front	Review	Classification	Date	Reference			Claims	KWOC	Draw Desc	Image
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☐ 16. Document ID: US 6690195 B1

L7: Entry 16 of 30

File: USPT

Feb 10, 2004

US-PAT-NO: 6690195

DOCUMENT-IDENTIFIER: US 6690195 B1

TITLE: Driver circuitry for programmable logic devices

Full	Title	Citation	Front	Review	Classification	Date	Reference			Claims	KWOC	Draw Desc	Image
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☐ 17. Document ID: US 6654346 B1

L7: Entry 17 of 30

File: USPT

Nov 25, 2003

US-PAT-NO: 6654346

DOCUMENT-IDENTIFIER: US 6654346 B1

**** See image for Certificate of Correction ****

TITLE: Communication network across which packets of data are transmitted according to a priority scheme

Full	Title	Citation	Front	Review	Classification	Date	Reference			Claims	KWOC	Draw Desc	Image
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☐ 18. Document ID: US 6605960 B2

L7: Entry 18 of 30

File: USPT

Aug 12, 2003

US-PAT-NO: 6605960

DOCUMENT-IDENTIFIER: US 6605960 B2

TITLE: Programmable logic configuration device with configuration memory accessible to a second device

Full	Title	Citation	Front	Review	Classification	Date	Reference			Claims	KWOC	Draw Desc	Image
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☐ 19. Document ID: US 6531889 B1

L7: Entry 19 of 30

File: USPT

Mar 11, 2003

US-PAT-NO: 6531889

DOCUMENT-IDENTIFIER: US 6531889 B1

TITLE: Data processing system with improved latency and associated methods

Full	Title	Citation	Front	Review	Classification	Date	Reference			Claims	KMC	Draw Desc	Image
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☐ 20. Document ID: US 6526461 B1

L7: Entry 20 of 30

File: USPT

Feb 25, 2003

US-PAT-NO: 6526461

DOCUMENT-IDENTIFIER: US 6526461 B1

TITLE: Interconnect chip for programmable logic devices

Full	Title	Citation	Front	Review	Classification	Date	Reference			Claims	KMC	Draw Desc	Image
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☐ 21. Document ID: US 6480027 B1

L7: Entry 21 of 30

File: USPT

Nov 12, 2002

US-PAT-NO: 6480027

DOCUMENT-IDENTIFIER: US 6480027 B1

TITLE: Driver circuitry for programmable logic devices

Full	Title	Citation	Front	Review	Classification	Date	Reference			Claims	KMMC	Draw Desc	Image
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☐ 22. Document ID: US 6467017 B1

L7: Entry 22 of 30

File: USPT

Oct 15, 2002

US-PAT-NO: 6467017

DOCUMENT-IDENTIFIER: US 6467017 B1

TITLE: Programmable logic device having embedded dual-port random access memory configurable as single-port memory

Full	Title	Citation	Front	Review	Classification	Date	Reference			Claims	KMMC	Draw Desc	Image
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☐ 23. Document ID: US 6466050 B1

L7: Entry 23 of 30

File: USPT

Oct 15, 2002

US-PAT-NO: 6466050

DOCUMENT-IDENTIFIER: US 6466050 B1

TITLE: Method to improve routability in programmable logic devices via prioritized augmented flows

Full	Title	Citation	Front	Review	Classification	Date	Reference			Claims	KMMC	Draw Desc	Image
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☐ 24. Document ID: US 6438737 B1

L7: Entry 24 of 30

File: USPT

Aug 20, 2002

US-PAT-NO: 6438737

DOCUMENT-IDENTIFIER: US 6438737 B1

** See image for Certificate of Correction **

TITLE: Reconfigurable logic for a computer

Full	Title	Citation	Front	Review	Classification	Date	Reference			Claims	KMMC	Draw Desc	Image
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☐ 25. Document ID: US 6373278 B1

L7: Entry 25 of 30

File: USPT

Apr 16, 2002

US-PAT-NO: 6373278

DOCUMENT-IDENTIFIER: US 6373278 B1

TITLE: LVDS interface incorporating phase-locked loop circuitry for use in programmable logic device

Full	Title	Citation	Front	Review	Classification	Date	Reference			Claims	KMC	Draw Desc	Image
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☐ 26. Document ID: US 6335636 B1

L7: Entry 26 of 30

File: USPT

Jan 1, 2002

US-PAT-NO: 6335636

DOCUMENT-IDENTIFIER: US 6335636 B1

TITLE: Programmable logic device input/output circuit configurable as reference voltage input circuit

Full	Title	Citation	Front	Review	Classification	Date	Reference			Claims	KMC	Draw Desc	Image
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☐ 27. Document ID: US 6252419 B1

L7: Entry 27 of 30

File: USPT

Jun 26, 2001

US-PAT-NO: 6252419

DOCUMENT-IDENTIFIER: US 6252419 B1

TITLE: LVDS interface incorporating phase-locked loop circuitry for use in programmable logic device

Full	Title	Citation	Front	Review	Classification	Date	Reference			Claims	KMC	Draw Desc	Image
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☐ 28. Document ID: US 6191607 B1

L7: Entry 28 of 30

File: USPT

Feb 20, 2001

US-PAT-NO: 6191607

DOCUMENT-IDENTIFIER: US 6191607 B1

TITLE: Programmable bus hold circuit and method of using the same

Full	Title	Citation	Front	Review	Classification	Date	Reference			Claims	KMC	Draw Desc	Image
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☐ 29. Document ID: US 6038400 A

L7: Entry 29 of 30

File: USPT

Mar 14, 2000

US-PAT-NO: 6038400

DOCUMENT-IDENTIFIER: US 6038400 A

TITLE: Self-configuring interface circuitry, including circuitry for identifying a protocol used to send signals to the interface circuitry, and circuitry for receiving the signals using the identified protocol

Full	Title	Citation	Front	Review	Classification	Date	Reference			Claims	KMC	Draw Desc	Image
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☐ 30. Document ID: US 5832240 A

L7: Entry 30 of 30

File: USPT

Nov 3, 1998

US-PAT-NO: 5832240

DOCUMENT-IDENTIFIER: US 5832240 A

TITLE: ISDN-based high speed communication system

Full	Title	Citation	Front	Review	Classification	Date	Reference			Claims	KMC	Draw Desc	Image
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